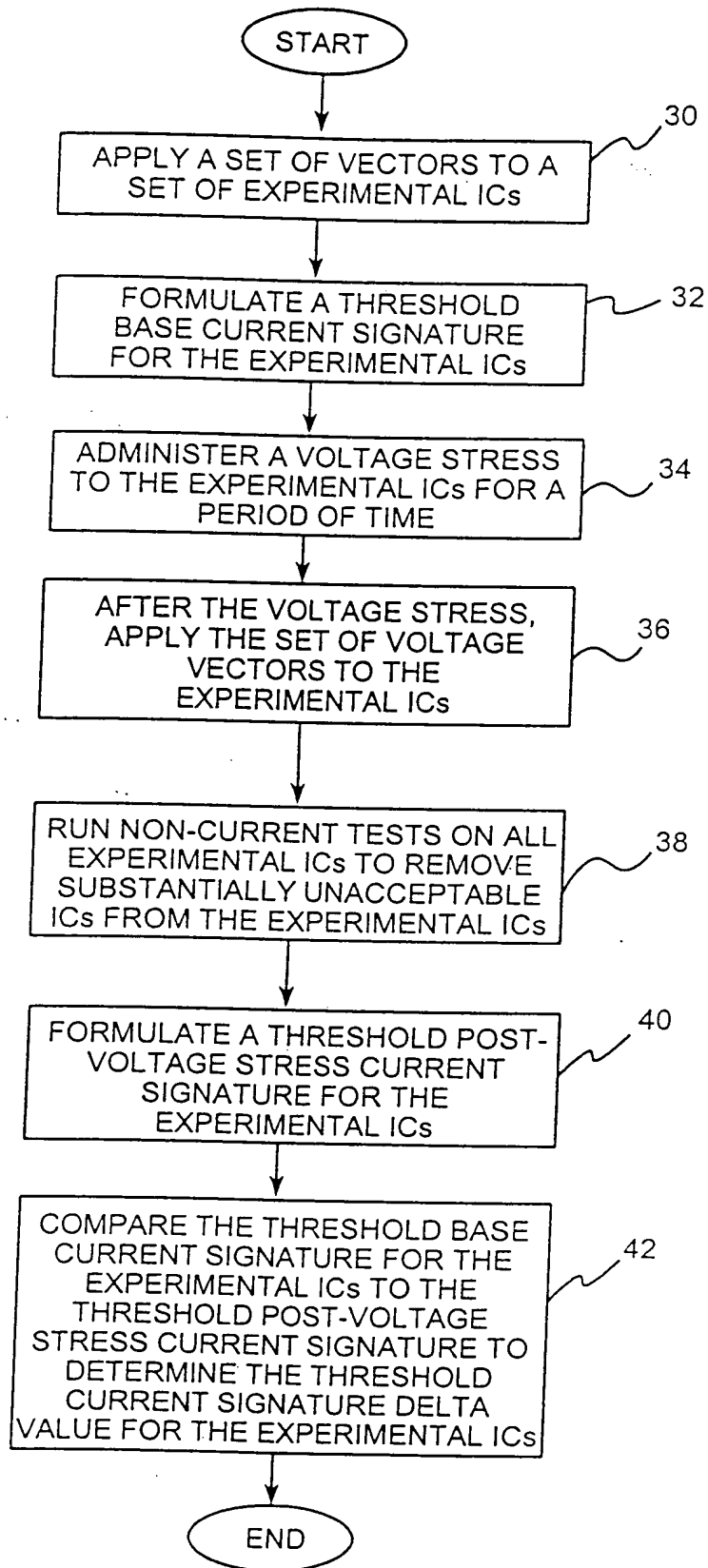


FIG. 1



*FIG. 2*

START

APPLY THE SET OF VOLTAGE  
VECTORS TO THE TEST  
INTEGRATED CIRCUIT AND A BASE  
CURRENT SIGNATURE IS  
FORMULATED FOR THE TEST  
INTEGRATED CIRCUIT

50

ADMINISTER VOLTAGE STRESS  
TO THE TEST INTEGRATED  
CIRCUIT

52

APPLY THE SET OF VOLTAGE  
VECTORS TO THE TEST  
INTEGRATED CIRCUIT AND  
FORMULATE A POST-STRESS  
CURRENT SIGNATURE

54

DETERMINE CURRENT SIGNATURE  
DELTA VALUES FOR THE TEST  
INTEGRATED CIRCUIT

56

END

FIG. 3

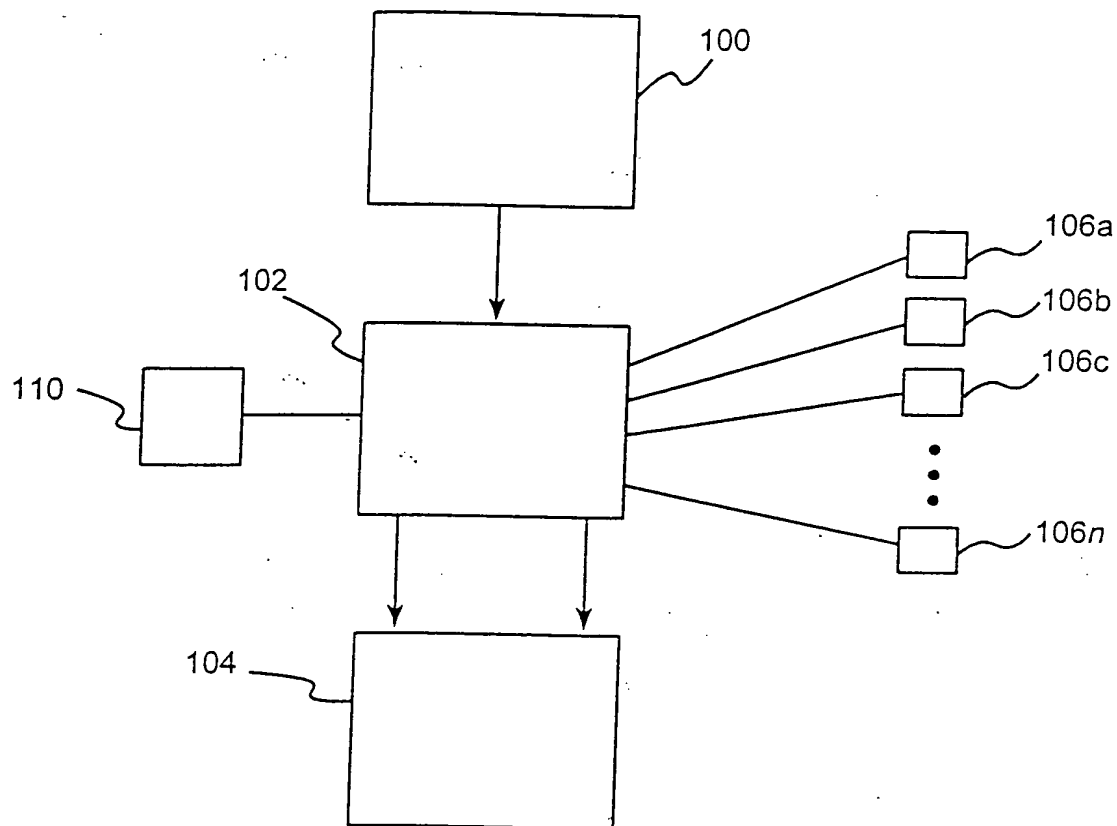


FIG. 4